STMicroelectronics, Inc.
1310 Electronics Drive
Carrollton, TX 75006-5039
Tel: 972-466-6000

September 24, 1998

Assistant Commissioner for Patents
Washington, D.C. 20231

Re: Inventor(s): Tsiu Chiu Chan, Arnaud Lepert, Lawrence Phillip Eng

For: Stacked Multi-Component Integrated Circuit Microprocessor

Our File No: 97-C-108

Sir:

Enclosed with this transmittal letter are:

(1) Subject patent application (26 pages) with Declaration and Power of Attorney;
(2) 2 sheets of informal drawings;
(3) Certificate of Express Mail;
(4) Assignment and Recordation Cover Sheet;
(5) Check in the amount of $830.00; and
(6) Return postcard which we would appreciate your date stamping and returning to us upon receipt.

The total filing fee has been calculated as follows:

Basic fee	=	$ 790.00
Recordation of Assignment	=	40.00
0 claim(s) in excess of 20	=	--
0 independent claim(s) in excess of 3	=	--
Total filing fee	=	$ 830.00

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Lisa K. Jorgenson
Reg. No. 34,845

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No. 97-C-108

In Re Application of:

Tsiu Chiu Chan, Arnaud Lepert, Lawrence Phillip Eng

For: **STACKED MULTI-COMPONENT INTEGRATED CIRCUIT MICROPROCESSOR**

CERTIFICATE OF MAILING 37 CFR 1.10

I hereby certify that the following correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" Service under 37 CFR 1.10 on the date indicated below and is addressed to: Assistant Commissioner for Patents, Box Patent Application, Washington, D. C. 20231, on Sept. 25, 1998:

1. Check in the amount of $830.00
2. Transmittal Letter
3. Declaration and Power of Attorney
4. Assignment and Assignment Cover Letter
5. Specification, Claims and Abstract consisting of 26 pages
6. 2 pages of informal drawings

Mary L. Kline
Signature of person mailing paper

Certificate No.: EE510175380 US

a:\certi

ST Docket No.: 97-C-108
Attorney Docket No.: 119932-1012

STACKED MULTI-COMPONENT INTEGRATED CIRCUIT MICROPROCESSOR

TECHNICAL FIELD OF THE INVENTION

This invention relates, in general, to the field of integrated circuits and, more particularly, to an apparatus and method for assembling integrated circuit microprocessors in a compact structure that maximizes spacial and manufacturing efficiency.

BACKGROUND

During the manufacture of integrated circuits, the processing of the semiconductor layers that form the circuitry of the integrated circuit is one of the most critical steps. In fact, as integrated circuit processor designs increase in complexity, the need to maximize the yield at every layering step becomes increasingly important.

Heretofore in this field, electronic systems such as computers, cellular telephones, etc., were built with individual components that were assembled on a circuit board. For example, an electronic system such as a computer generally includes a microprocessor, an input/output or bus interface, a memory cache, keyboard control circuits, video circuits, and a floppy disk drive, hard disk drive and/or CD-ROM control circuits. The central component of the electronic system is the processor, now generally called a microprocessor to indicate the decreasing size of the individual electronic components.

Using the microprocessor that forms part of the electronic system, as an example, it can be observed that the following evolution has occurred. The creation of the logic that forms the main component of the microprocessor on a single silicon substrate was a first step. A second step was to decrease the distance between the logic of the processor

and the bit buffering components that the microprocessor uses to control processor flow by creating a single chip containing the microprocessor and a cache memory. A third step was the integration of a microprocessor, cache memory and an input/output bus interface, also on a single chip.

United States Letters Patent No. 5,561,594, issued October 1, 1996 (SGS-Thomson Microelectronics, Ltd.) discloses an electrical assembly in which the electrical component is mounted on a multi-layer printed circuit board having a plurality of conducting pins located in perforations within the board. The conducting pins located in the board have pointed ends that project above the board and make electric contact with solder bumps on the electrical component. The specification describes an apparatus and method for flip-chip packaging. As with conventional manufacturing, the printed circuit board has standard size vias that are drilled through for each individual substrate.

United States Letters Patent No. 5,621,193, issued April 15, 1997 (Northrop Grumman Corp.) discloses a method for electrically connecting surface conductors to edge conductors by use of an intersecting side non-conductor substrate having a through hole in the substrate and metalization of the through hole. The electrical connections between the surface

and the side include forming an intersecting ceiling plug in the via prior to cutting the intersecting side.

SUMMARY OF THE INVENTION

It has been recognized herein that a need has arisen for a simple, effective apparatus and method for providing a high frequency microprocessor that can be developed using present processing equipment, materials and techniques. The need has also arisen for a more versatile microprocessor design for medium to high performance semiconductors, using current substrates and methods of manufacturing substrates with increased efficiency and decreased cost. Furthermore, a need has arisen for a substrate that can be made using present equipment and using standard manufacturing techniques, but which decreases the total number of layers deposited and etched on a monolithic substrate.

The present invention provides a simple, effective apparatus and method for designing, producing and packaging high performance ultra large scale integration (ULSI) semiconductor integrated circuits. The present invention can increase the efficiency of the production in manufacture of semiconductor integrated circuits. The present invention can also decrease the processing time and materials needed to manufacture ULSI semiconductor integrated circuits.

One embodiment of the present invention is a microprocessor including a first integrated circuit chip, having an active face including a central processing unit, and

a second integrated circuit chip electrically connected to the active face of the first integrated circuit chip. The second integrated circuit chip provides added functionality to the central processing unit of the first integrated circuit chip. Examples of central processing units for use with the present invention are digital signal processors or field programmable gate arrays.

The second integrated circuit chip adds functionality to the first integrated circuit chip by, for example, providing accessible memory or a cache, such as a level 1 or 2 cache, at a short distance without the need for long routing lines within the substrate of the first integrated circuit chip. Examples of memory chips that can be used include but are not limited to: DRAM, SRAM or FLASH. Alternatively, the second integrated circuit chip can be an analog-to-digital converter or a digital-to-analog converter.

More particularly, the present invention has a first integrated circuit chip that is used as a base to support another integrated circuit chip, such as a memory circuit. A third integrated circuit chip may also be disposed adjacent to the second integrated circuit chip. In one embodiment, the second integrated circuit is "piggybacked" onto the first integrated circuit by flipping it so that the active

components of the integrated circuit are exposed and available to make contact with the first integrated circuit chip.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the features and advantages of the present invention, reference is now made to the detailed description of the invention along with the accompanying figures in which corresponding numerals in the different figures refer to corresponding parts and in which:

Figure 1 is an isometric view of a microprocessor of the present invention;

Figure 2 is a side view of a microprocessor according to another embodiment of the present invention; and

Figure 3 is a close-up side view of a microprocessor contact.

DETAILED DESCRIPTION OF THE INVENTION

While the making and using of various embodiments of the present invention are discussed in detail below, it should be appreciated that the present invention provides many applicable inventive concepts which can be embodied in a wide variety of specific contexts. The specific embodiments discussed herein are merely illustrative of specific ways to make and use the invention and do not delimit the scope of the invention.

Integration of ultra large scale integrated (ULSI) circuits comes in the form of, for example, the Cyrix 6x86MX. This integrated microprocessor incorporates the following electronic components into a single chip: a Bus interface, a memory management unit, a control unit, code and data cache, line cache, prefetching IF, instruction decode, v- and u-pipes, Registers, a floating processor unit and other components.

The large scale integration of ULSI components has led to a number of packaging problems and limitations. One such case is the embedding of a large memory core (like a DRAM) in a microprocessor or other processing logic such as field programmable gate arrays (FPGA), one example of which is a large application specific integrated circuit (ASIC) or sub-system. To integrate these different electronic components,

the chip must be manufactured using a diverse mix of integrated circuit processing technologies, namely, those to manufacture a processor and those to manufacture memory. As the different electronic components of the processor require deposition of different layers, materials, etching, etc., on a single wafer, the problem of integrating a larger number of electronic components having smaller electrical components is increased geometrically. For a microprocessor, one example of combination processing is the formation of DRAM followed by the formation of ASIC components. Similar examples include the combination of a FLASH or SRAM memory formation process, followed by an ASIC process or vice-versa. Unfortunately, this mixing of technologies requires a compromise from each of the components used.

For example, a DRAM process that is specifically customized for creating DRAM cells, presently requires 2-4 polysilicon layers and typically 1-2 metal layers. An SRAM forming process will be customized accordingly, requiring 2-4 polysilicon layers and 2-3 metal layers. An ASIC process is one designed to support microprocessors specifically built for a particular logic and can be composed of 1 polysilicon and 4-5 metal layers. A combination of such electronic components, even when maximizing the efficiency of embedding like components of a DRAM and microprocessor unit, requires from

between 2 to 4 poly silicon layers and 4 to 5 metal layers. To satisfy the requirements necessary to build a DRAM memory cell including the extensive interconnections, requires, at this level of integration, to route multiple address lines and data busses from the many cells to the microprocessor.

The present inventors have recognized the limitations of cost and performance of merging the functions of a microprocessor and, e.g., DRAM, SRAM or embedding memories on a single monolithic chip. The problem can be further illustrated by the use of multi-chip carriers for the Pentium microprocessor or the circuit board for the Pentium II in which all the electronic components are embedded in a single monolithic chip.

While a number of processing solutions have provided cost-effective methods to produce higher levels of integrations on a single chip, combination microprocessors have reduced performance over what could otherwise be obtained from a monolithic solution, if such were available.

Turning now to the present invention, Figure 1 is an isometric view of an integrated circuit microprocessor generally depicted as 10. The integrated circuit microprocessor 10 has a first integrated circuit chip 12, shown here with the active components 30 and the backside of the silicon not having any active circuit disposed thereon

face down. The amount and types of electronic circuits that are disposed as active components 30 integral with integrated circuit chip 12 will depend on the specific logic processor required. Types of integrated circuits that may be used include the logic necessary to provide a central processing unit, such as, a digital signal processor or an ASIC processor.

A second integrated circuit chip 14 is depicted connected to integrated circuit chip 12. Extending from the integrated circuit chip 12, and being integral therewith, are electrical contacts 16. Electrical contacts 16 generally rise from the integrated circuit chip 12 surface and are used to connect active components 30 of the integrated circuit chip 12 with active components (not depicted) integral with the second integrated circuit chip 14. One aspect of the present invention that is apparent from the isometric view is that the distance between connections among active components on the chips 12 and 14 is greatly reduced by not having a connector, such as wire bonding or solder balls or columns between the first and second integrated circuit chips 12, 14. The distance between the chips 12, 14 can be about that of a micro-solder ball. Generally, solder balls range in size from about 8 to 200 microns in thickness.

The electrical contacts 16 form an electrical connection with the electrical contacts 18 of integrated circuit chip 14, e.g., by bump bonding or by solder reflow of metalization layers (described hereinbelow). The electrical contacts 18 of the second integrated circuit chip 14 can also be integral with the second integrated circuit chip 14 and electrically connect to its active components. Finally, disposed on the same surface of the integrated circuit chip 12 as the electrical contacts 16, are pads 20 that serve to connect the integrated circuit microprocessor 10 with a mother or sister-board.

Figure 2 is a cross-sectional side view of an integrated circuit microprocessor 10 made in accordance with the present invention. In order to provide for the electrical connection of the integrated circuit microprocessor 10, the pads 20 are located so as to permit the deposition of solder balls, solder columns or connection by wire bonding for connection with, e.g., a printed circuit board such as a mother or sister board. To do so, the size of the second integrated circuit chip 14 is less than the size of the integrated circuit chip 12. Alternatively, the second integrated circuit chip 14 can be offset sufficiently from the top surface of the integrated circuit chip 12 to provide for an opening through which connections from pads 20 may be made.

As seen from the side view of figure 2, the electrical contacts 16 and 18 are integral with the integrated circuit chips 12, 14 and 15. The electrical contacts 16, 18 are disposed on the face containing active components 30 and 32 of the chips 12, 14 and 15. By positioning integrated circuit chips 14 and 15 in such close proximity to the active components of the integrated circuit chip 12, the distance that electrical signals must travel between active components 30 and 32 is greatly reduced in comparison to placing the equivalent circuit on real estate adjacent the processor logic on a monolithic chip. Furthermore, the number of reroute lines, such as route address lines and data bus lines, occupying real estate on the active surface of the chip 12 and chips 14 and 15 are reduced.

Also, by positioning a separate integrated circuit that adds functionality to the first integrated circuit, such as providing additional local FLASH memory, an L1 or L2 cache, or a digital-to-analog converter, the ancillary or complementary features and functionality of integrated circuit microprocessor 10 can be changed without having to completely redesign the active components of the microprocessor. For example, different memory capacities can be positioned on the integrated circuit chip 12 through contacts designed at the same position.

The present invention maximizes the efficiency of the creation of the individual components of a microprocessor by permitting the manufacturer to optimize the processing steps, and consequently the quality, of the different components. For example, the first integrated circuit chip 12 can have disposed thereon only a central processing unit. Memory that is rapidly accessible to the central processing unit can be disposed directly thereon in the form of the second integrated circuit chip 14, as can other functionalities such as audio or video processors.

Yet another advantage of the present invention is the recognition that the components that make up these "ancillary" functionalities can change over time. The present invention permits for the rapid replacement, in the microprocessor assembly line, of old outdated components for new components. The replacement of ancillary components can occur without the need to change the original design of the integrated circuit microprocessor to accommodate the new functionality. The present invention also eliminates the need to completely redesign the entire surface of a monolithic fully integrated chip as is presently done, as the new updated components can be piggy-backed directly on chips with pre-existing designs.

A problem with variable heating within combination microprocessors on monolithic chips has been encountered. By

using separate integrated circuit units, the variance in the power requirements and, consequently, the heat production of a single monolithic chip, having a wide array of different functionalities, may be reduced.

Figure 3 is a close-up of one electrical contact 18 for use with the present invention. The active components 32 of the integrated circuit chip 14 are depicted in this cross-section as separated by a dielectric or electrically insulative layer 24. Disposed on the insulative layer 24 is patterned a metalization layer 26 that provides for isolated electrical contacts between the integrated circuit chips 12 and 14. The metalization layer 26 connects to the active components 32 of chip 14 by having an electrical connection (not depicted) that crosses insulative layer 24. To provide an integral contact, a rise 22 that is either insulative or conductive, can be deposited on the insulative layer 24. The rise 22 can also be coated with the metalization 26. Finally, a bonding layer 28 can be disposed on the metalization 26. The deposited bonding layer 28 (as opposed to adding connectors such as wire bonding or solder balls) can be, e.g., gold, tin, iridium, copper, or combinations thereof. The bonding layer 28 provides a direct connection of metalization layers 26 on the active faces of the integrated circuit chips by having an electrical contact between the electrical

contacts 16 and 18. By a direct connection it is meant that the connection between metalization 26 and the adjacent integrated circuit chip does not require and intermediate electrically conductive component, e.g., a solder ball. The bonding layer 28 can also be thermocompressible to provide for a mechanical bond between the contacts 16 and 18. The mechanical bond helps to retain, e.g., the second integrated circuit chip 14 on the integrated circuit chip 12, whether or not the integrated circuit chips 12 and 14 are further packaged or encapsulated.

The invention disclosed here allows for optimization of cost and performance of individual components to develop an electronic system or sub-system. Accordingly, in one embodiment the present invention includes combining a microprocessor with a separate memory, such as DRAM. The microprocessor can be manufactured in a process with a high level of interconnects, such as having 4 to 5 metal layers. Likewise, memory can be produced and the process of its production optimized.

The present invention has the following advantages. First, it combines two or more integrated circuits into a more compact structure over chip carriers (packaging solutions) or printed circuit boards. It also allows individual components, such as the microprocessor's CPU and the memory or cache, to

be manufactured using processes and technology that optimize the speed, performance and cost of that component. Furthermore, the invention allows higher integration of components that otherwise might be limited.

The present inventors have solved the problem posed by the limits imposed by the monolithic embedding of circuits, such as embedded applications. By emphasizing the efficiency of production of individual components the assembly process need only be expanded to support the packaging requirements of the individual components.

The present invention also improves the performance of the functional components that comprise the overall microprocessor by eliminating packaging or wiring delays by having direct contact between the integrated circuit processor and ancillary components. It is expected that using the present invention, high frequencies in the 500 Megahertz to 7 Gigahertz can be supported and achieved.

While this invention has been described in reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is

therefore intended that the appended claims encompass any such modifications or embodiments.

What is claimed is:

1. A microprocessor comprising:

a first integrated circuit chip having an active face including a central processing unit; and

a second integrated circuit chip mounted on, and electrically connected to, the active face of the first integrated circuit, wherein the second integrated circuit chip provides added functionality to the central processing unit of the first integrated circuit.

2. The microprocessor of claim 1, wherein the central processing unit comprises a digital signal processor.

3. The microprocessor of claim 1, wherein the central processing unit comprises a field programmable gate array.

4. The microprocessor of claim 1, wherein the second integrated circuit chip comprises memory.

5. The microprocessor of claim 4, wherein the memory comprises cache.

6. The microprocessor of claim 4, wherein the memory comprises DRAM.

7. The microprocessor of claim 4, wherein the memory comprises SRAM.

8. The microprocessor of claim 4, wherein the memory comprises FLASH.

9. The microprocessor of claim 1, wherein the second integrated circuit chip comprises an analog-to-digital converter.

10. The microprocessor of claim 1, further comprising a third integrated circuit chip adjacent the second integrated circuit chip wherein the third integrated circuit chip adds further functionality to the integrated circuit microprocessor.

11. The microprocessor of claim 1, wherein the electrical connection between the first integrated circuit chip and the second integrated circuit chip is by direct connection of metalizations on the active faces of the first and second integrated circuit chips by a bonding layer.

12. The microprocessor of claim 1, wherein the first and second integrated circuit chips are further defined as having

a profile, and wherein the profile of the second integrated circuit chip is less than the profile of the first integrated circuit chip.

13. A microprocessor comprising:

a first chip having an active face including a central processing unit; and

a second chip having an active face, the second chip mounted on, and electrically connected to, the active face of the first chip, wherein the second chip adds functionality to the central processing unit of the first chip and wherein the electrical connection is by a bonding layer between metalization that is integral with the active faces of the first and second chips.

14. The microprocessor of claim 13, wherein the central processing unit comprises a digital signal processor.

15. The microprocessor of claim 13, wherein the central processing unit comprises a field programmable gate array.

16. The microprocessor of claim 13, wherein the second chip comprises memory.

17. The microprocessor of claim 13, wherein the second chip comprises an analog-to-digital converter.

18. The microprocessor of claim 13, further comprising a third chip adjacent the second chip wherein the third chip adds further functionality to the integrated circuit microprocessor.

19. The microprocessor of claim 13, wherein the first and second integrated circuit chips are further defined as having a profile, and wherein the profile of the second integrated circuit chip is less than the profile of the first integrated circuit chip.

20. A method for creating an integrated circuit microprocessor comprising the steps of:

obtaining a first chip with an active surface including a central processing unit having a metalization and a bonding layer;

obtaining a second chip having a different functionality from the first chip, the second chip having a metalization and a bonding layer;

mounting the second chip on the active surface of the first chip; and

electrically connecting the first and second chips by electrically connecting the bonding layers on the metalization.

STACKED MULTI-COMPONENT INTEGRATED CIRCUIT MICROPROCESSOR

ABSTRACT OF THE DISCLOSURE

An apparatus and method for fabricating a microprocessor comprising a first chip (12) having an active face (30) including a central processing unit and a second chip (14) having an active face (32) electrically connected to the active face of the first chip (12), wherein the second chip (14) provides added functionality to the central processing unit of the first chip (12) and wherein the electrical connections (16, 18) are through bonding layers (28) that are in contact with the metalization 26 on the first and second chips (12, 14), is disclosed.

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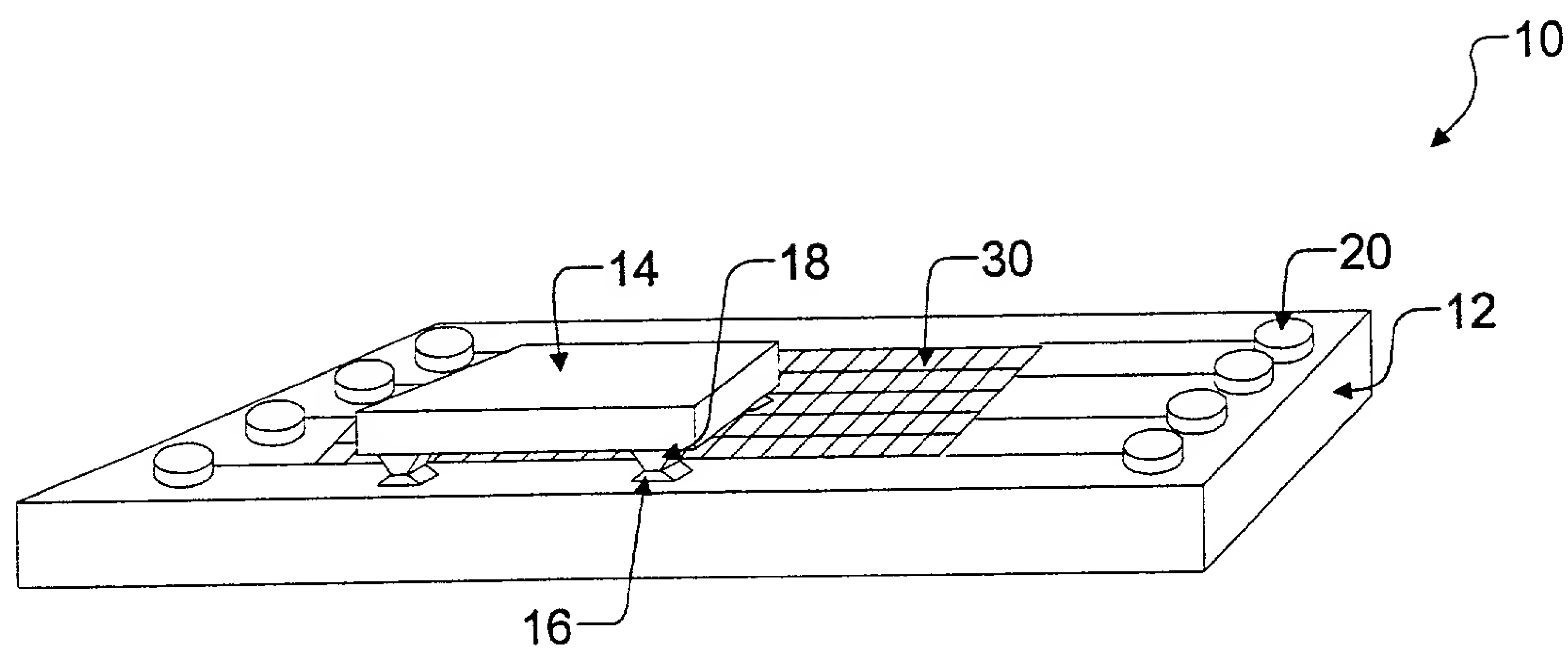

Figure 1

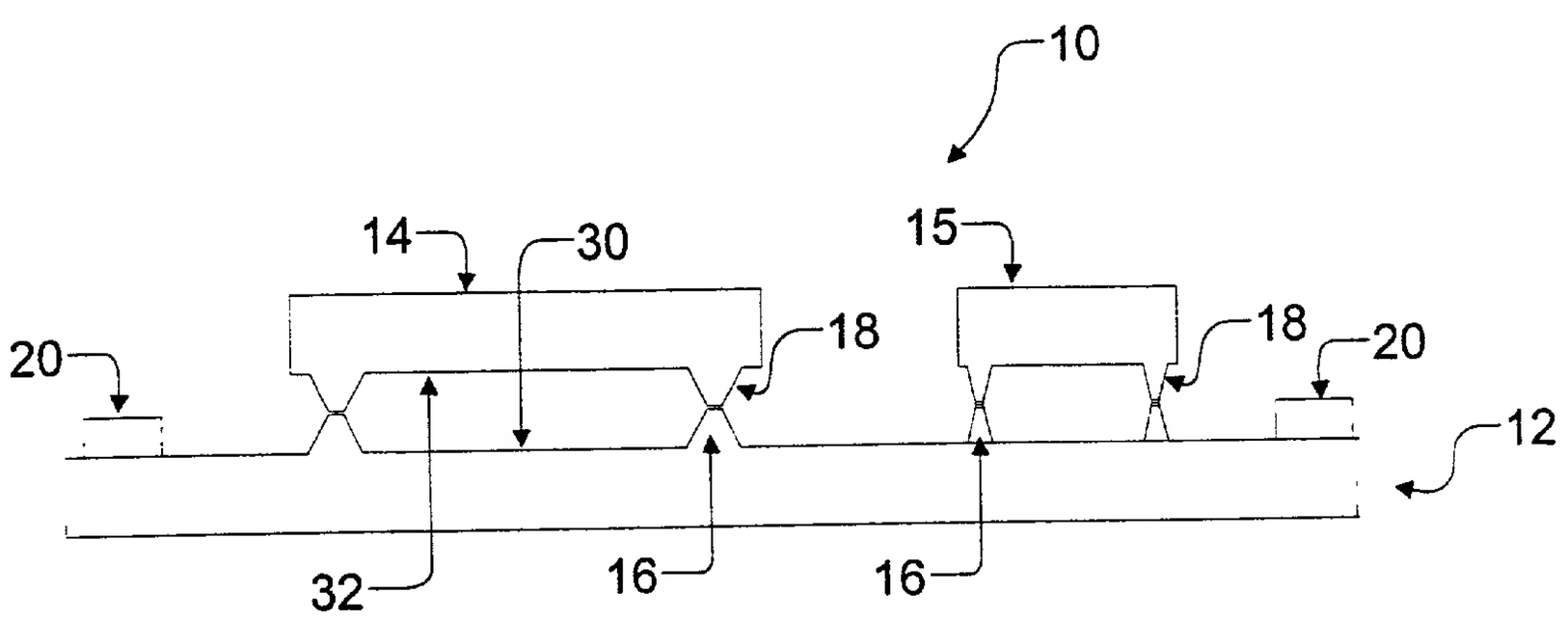

Figure 2

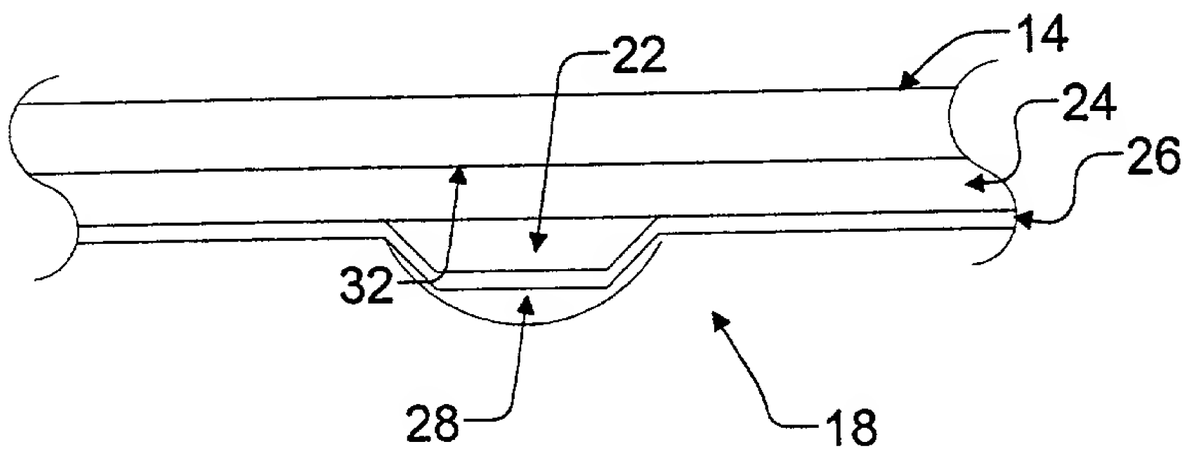

Figure 3

Docket No.: __97-C-108_

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

STACKED MULTI-COMPONENT INTEGRATED CIRCUIT MICROPROCESSOR

the specification of which (check one)

_X_ is attached hereto.

_____ was filed on _____ as United States Application Serial No. _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application as defined in Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Benefits Claimed?
_____ (Appl. No.)	_____ (Country)	_____ (Filing Date)	__ Yes __ No
_____ (Appl. No.)	_____ (Country)	_____ (Filing Date)	__ Yes __ No
_____ (Appl. No.)	_____ (Country)	_____ (Filing Date)	__ Yes __ No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information material to the patentability of this application as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Application(s)

(Application Serial No.)	(Filing Date)	(Status - patented, pending, abandoned)

I hereby appoint Theodore E. Galanthay, Reg. No. 24,122, Lisa K. Jorgenson, Reg. No. 34,845 Mark E. McBurney, Reg. No. 33,114; Robert D. McCutcheon, Reg. No. 38,717; Sanford E. Warren, Jr., Reg. No. 33,219; Daniel F. Perez, Reg. No. 33,755; and Edwin S. Flores, Reg. No. 38,453 as my principal attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

Send Correspondence To:
Lisa K. Jorgenson
STMicroelectronics, Inc.
1310 Electronics Dr.
Mail Stop 2346
Carrollton, TX 75006

Direct Telephone Calls To: Lisa K. Jorgenson at telephone number (972) 466-7414.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Inventor: Tsiu Chiu Chan

Signature: Tsiu Chiu Chan

Date of Signature: Sept 25, 98

Residence: 1633 Camero Drive
Carrollton, TX 75006

Citizenship: U.S.A.

Post Office
Address: Same as residence address

Inventor: Arnaud Lepert

Signature:

Date of Signature: 9-11-1998

Residence: Apt. 16, 92 rue Louis Neel
F-38330
Montbonnot, FRANCE

Citizenship: French

Post Office
Address: Same as residence address

Inventor: Lawrence Philip Eng

Signature:

Date of Signature: Sep 25, 1998

Residence: 3315 Water Oak
Dallas, TX 75234

Citizenship: U.S.A.

Post Office
Address: Same as residence address